ABSTRACT

Providing a CDR circuit having a stable clock extracting function and a data regenerating function with a high-speed data input process by reducing the operation speed of the phase comparator circuit. With a phase comparator circuit capable of operating with a clock signal whose period is 2 times the unit time width of the inputted data signal, the pulse width of the phase error signal, representing the difference in phase between the transition point of the data signal and the transition point of the clock signal, is extended as much as the unit time width of the data signal.